

CUST#089002

NPOWEME-P0021-USA-1/再審初稿/柯慧琦

AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A structure of an embedded channel write/erase flash memory cell,
 5 comprising mainly:
 an N-substrate;
 a flash memory cell region comprising mainly:
 [[and]]
 a deep P-well formed [[on]] in said substrate;
 10 an N-well formed [[on]] in said deep P-well, a
 deep [[P-type]] p-type region and a shallow
 p-type region being implanted in
 predetermined positions of said N-well;
 [[and]]
 15 a first n-type region formed at one side of said
 shallow p-type region and in said deep p-type
 region in said N-well to be used as a drain;
 a second n-type region formed at the other side
 of said shallow p-type region in said N-well
 20 to be used as a source; and
 a stacked gate formed on said N-well; and
 a CMOS device region comprising mainly:
 a first deep P-well formed [[on]] in said
 substrate;
 25 a first N-well formed [[on]] in said first deep
 P-well, a plurality of p-type regions being
 implanted in predetermined positions of said
 first N-well;
 a second deep P-well formed [[on]] in said
 30 substrate; and
 a second N-well formed [[on]] in said second deep
 P-well, a plurality of p-type regions being

CUST#089002

NPO#EME-P0021-USA-1/再審初稿/柯慈琦

implanted in pre determined positions of said
second N-well.

5 Claim 2 (original): The structure of an embedded channel
write/erase flash memory cell as claimed in claim 1,
wherein an oxide layer is further provided between said
N-well and said stacked gate of said flash memory cell
region.

10 Claim 3 (original): The structure of an embedded channel
write/erase flash memory cell as claimed in claim 2,
wherein a smiling effect pattern is caused by oxidation
between said stacked gate and said oxide layer.

15 Claim 4 (canceled)

20 Claim 5 (original): The structure of an embedded channel
write/erase flash memory cell as claimed in claim 1,
wherein the implanted depth of said deep p-type region
in said N-well of said flash memory cell region is larger
than that of said shallow p-type region.

25 Claim 6 (original): The structure of an embedded channel
write/erase flash memory cell as claimed in claim 1,
wherein said deep p-type region in said N-well of said
flash memory cell region is connected with one end of
said shallow p-type region.

30 Claim 7 (canceled)

Claim 8 (currently amended): The structure of an
embedded channel write/erase flash memory cell as

CUST#089002

NPO#EME-P0021-USA-1/再審初稿/柯建琦

claimed in claim [[7]] 1, wherein a field oxide layer and an n-type ion channel barrier layer can also be provided between said second n-type region and said shallow p-type region in said N-well, said n-type ion channel barrier layer being disposed below said field oxide layer.

Claim 9 (currently amended): The structure of an embedded channel write/erase flash memory cell as claimed in claim [[14]] 1, wherein said first n-type region implanted in said deep p-type region of said flash memory cell region is connected to said deep p-type region via an electrical short circuit.

Claim 10 (currently amended): The structure of an embedded channel write/erase flash memory cell as claimed in claim 9, wherein said electrical short circuit is formed by using a metal contact to penetrate a junction [[of]] between said first n-type region in said deep p-type region and said deep p-type region.

Claim 11 (currently amended): The structure of an embedded channel write/erase flash memory cell as claimed in claim 9, wherein said electrical short circuit is formed by using a metal contact to connect said exposed first n-type region in said deep p-type region with said deep p-type region.

Claim 12 (canceled)

Claim 13 (currently amended): The structure of an embedded channel write/erase flash memory cell as

CUST#089002

NPO#EME-P0021-USA-1/再審初稿/柯慈琦

claim d in claim 1, wherein said CMOS device region further comprises a first P-well formed [[on]] in said substrate and at one side of said first deep P-well.

5 Claim 14 (currently amended): The structure of an embedded channel write/erase flash memory cell as claimed in claim 13, wherein said CMOS device region further comprises a second P-well formed on said substrate and at one [[said]] side of said first P-well.

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Claim 15 (currently amended): The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein said CMOS device region further comprises a first P-well formed [[on]] in said first deep P-well.

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Claim 16 (currently amended): The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein said CMOS device region further comprises a second P-well formed [[on]] in said second deep P-well.

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